

REMARKS

The Examiner's Office Action of July 9, 2003 has been received and its contents reviewed. Applicant would like to thank the Examiner for the consideration given to the above-identified application, and for indicating that claim 3 contains allowable subject matter.

Claims 2-9 are pending for consideration, of which claim 7 is independent.

Referring now to the detailed Office Action, claims 2, 7 and 8 stand rejected under 35 U.S.C. §102(e) as anticipated by Wang et al. (U.S. Patent NO. 6,429,116 – hereafter Wang). Further, claims 4, 5, 6, and 9 stand rejected under 35 U.S.C. §103(a) as unpatentable over Wang. Finally, claim 3 stands objected to as dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. These rejections and objection are respectfully traversed at least for the reasons provided below.

Before discussing Wang in detail, Applicant would like to summarize and clarify the features of the presently claimed invention using reference numerals and exemplary drawings in the specification.

The features of claim 7 of the present invention reside in a method for fabricating a semiconductor device comprising the steps of:

- (a) forming, on a substrate (100), a first insulating film (101) with a relatively low dielectric constant and low mechanical strength;
- (b) partially retaining the first insulating film (101) in a first region through selective etching using a first mask pattern (102) formed on the first insulating film (101);
- (c) forming a second insulating film (103) with a relatively high dielectric constant and high mechanical strength, such that the second insulating film (103) covers the retained first insulating film (101);
- (d) forming a thinned portion of the second insulating film (103) on the retained first insulating film (101) by planarizing the second insulating film (103) by polishing;
- (e) forming a first interconnect groove (105) in the thinned portion of the second insulating film (103) and the retained first insulating film (101) through selective etching the thinned portion of the second insulating film (103) and the retained first insulating film (101) using a second mask pattern (104) formed on the thinned portion of the second insulating

film (103) (as shown in, e.g., Fig. 2C); and

- (f) forming a buried interconnect (107) in the first interconnect groove (105),
- (g) wherein the thinned portion of the second insulating film 103) and the retained first insulating film (101) are provided on the sides of the buried interconnect (107) (as shown in, e.g., Fig. 3B).

Accordingly, since the first insulating film that has a low mechanical strength is not exposed during the planarization of the second insulating film of high mechanical strength by polishing, defects such as peeling and scratching of the first insulating film can be prevented.

In addition, since the buried interconnect is formed by filling the metal film in the first interconnect groove formed in the first insulating film with a low dielectric constant, the first insulating film can be disposed between the interconnects, even if the interconnect pitch is small.

Turning now to Wang, the reference teaches a method for forming a Dual Damascene interconnect structure including the steps of:

- (a) forming, on a substrate, a first insulating film (24) with a relatively low dielectric constant and low mechanical strength;
- (b) partially retaining the first insulating film (24) in a first region through selective etching using a first mask pattern (28) formed on the first insulating film (24), and forming a slot via (50) in the first insulating film (24);
- (c) filling the slot via (50) with a second insulating film (30) by forming the second insulating film (30) with a relatively high dielectric constant and high mechanical strength, such that the second insulating film (30) covers the retained first insulating film (24);
- (d) forming a thinned portion of the second insulating film (30) on the retained first insulating film (24) by planarizing the second insulating film (30) by polishing;
- (e) forming a trench (38) and a re-opened via (36) in the thinned portion of the second insulating film (30) and the second insulating film (30) refilling the slot via (50) through selective etching using a second mask pattern (34) formed on the thinned portion of the second insulating film (30) (see Fig. 8); and
- (f) forming an underlying conductive line (42) and a stud (40) in the trench (38) and the re-opened via (36),

(g) wherein the thinned portion of the second insulating film (30) is provided on the sides of the underlying conductive line (42) (see Fig. 11).

According to step (e) of Wang, after forming the trench (38) by etching the thinned portion of the second insulating film (30), the re-opened via (36) is formed by etching the second insulating film (30) refilling the slot via (50) provided directly below the trench (38). Hence, etching is performed on the second insulating film (30) in the slot via (50) but not on the first insulating film (24) (as disclosed in column 8, lines 5-9).

In addition, according to Wang, only the second insulating film (30) is provided on the sides of the underlying conductive line (42), while the first insulating film (24) is provided on the bottom and not the sides of the underlying conductive line (42) (see Fig. 12).

On the other hand, according to step (e) of the present invention, the first interconnect groove (105) is formed by selective etching of the thinned portion of the second insulating film (103) and the retained first insulating film (101). Hence, the retained first insulating film (101) is also being etched.

Moreover, according to the presently claimed invention, the thinned portion of the second insulating film (103) and the retained first insulating film (101) are provided on the sides of the buried interconnect (107).


For the foregoing reasons, claim 7, as well as its dependent claims, is clearly distinguishable over Wang, and the §102(e) rejection is insupportable.

With respect to the §103(a) rejection, the arguments set forth above in relation to the §102(e) rejection of claims 2, 7, and 8 are also applicable to the §103(a) rejection of dependent claims 4, 5, 6, and 9.

In view of the amendments and arguments set forth above, Applicant respectfully requests reconsideration and withdrawal of all the pending rejections and objection.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicant's representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Respectfully submitted,


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